

## Abstract

### Optimized bus connection for acceptance of bus transactions

For optimization of the mode of operation of processor systems, there is proposed a bus connection which divides bus transactions substantially into transactions that must be executed in strictly logical sequence and that do not have to be executed in strictly logical sequence. Subsequently the transactions are again arrayed one after another in serial manner for further processing, with the feature that, in given cases, transactions that do not have to be executed in strictly logical sequence are moved ahead of transactions that must be executed in strictly logical sequence. The result is a gain in time and thus performance for the processor system.

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